CS420/520 FINAL Coverage

1. Pipelining
   1.1 Pipelining datapath design & control
      1.1.1 latch registers & execution unit
      1.1.2 control station
   1.2 Pipelining performance
      1.2.1 Comparison to single cycle and multi-cycle machines (related to Clock cycle time, CPI, etc.)
   1.3 Pipelining hazards
      1.3.1 classifications and examples
      1.3.2 solutions to structural hazards
      1.3.3 solutions to data hazards; forwarding / bypassing
      1.3.4 solutions to control hazards; hardware change, BDS, etc
      1.3.5 impact of hazards on pipelining performance
      1.3.6 delay load and load interlock control
   1.4 instruction level parallelism
      1.4.1 data dependence and name dependence (RAW, WAR, WAW)
      1.4.2 software instruction scheduling/re-ordering
      1.4.3 register renaming

2. Memory hierarchy
   2.1 Motivations of caches; Locality principals
   2.2 Concept of block, set, set index, cache size, etc
   2.3 Cache organizations and cache size calculations
   2.4 Placement issues
   2.5 Identification/location issues
   2.6 Replacement issues, LRU, NRU
   2.7 Writing issues
   2.8 3C misses
   2.9 multi-level caches, local and global cache miss rate and miss penalty
   2.10 impact of cache designs on computer performance
   2.11 Memory interleaving for reducing miss penalty
   2.12 performance and trade-offs

3. I/O systems
   3.1 3-stage access in magnetic disks
   3.2 reliability and availability
   3.3 RAID
   3.4 bus types and bus hierarchy
   3.5 OS’s responsibility in I/O systems, interrupt, DMA

Reading:
Review textbooks based on lecture notes
Re-do homework assignments and lecture examples